REMARKS

Claims 1-27 are now pending. No claims stand allowed.

Claims 1-18 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. New claims 19-27 have been added by this amendment and also particularly point out and distinctly claim subject matter regarded as the invention. The amendment also contains minor changes of a clerical nature. No "new matter" has been added by the amendment.

The specification has been amended to correct informalities noted by the Examiner in the Office Action and otherwise. These corrections are of a clerical nature and do not add "new matter".

Objection to Specification

The specification stands objected to for alleged informalities that much of the subject matter disclosed from page 10, line 9 to page 11 (last line) essentially repeats information already set forth previously. This objection is respectfully traversed.

In the present specification, as amended, the description from page 10, line 9 to page 11 (last line) describes a system for maintaining TLB coherency in a computer system in accordance with one embodiment of the present invention, while the previous description from page 8, line 21 to page 10, line 9 describes a method for maintaining TLB coherency in computer systems in accordance with one embodiment of the present invention. Thus, although the description may appear similar, the subject matter thereof is directed to a different aspect of the present invention from that of the previous

description. Accordingly, the description is not unnecessary. It is respectfully requested that the objection be withdrawn.

Claim Objections

Claims 1-8 and 10-18 stand objected to because of certain alleged informalities. The claims have been amended to eliminate the alleged informalities in accordance with the Examiners suggestion. With this amendment, it is respectfully requested that the objection to the claims be withdrawn.

The 35 U.S.C. §112 Rejection, Second Paragraph

Claims 12-18 stand rejected under 35 U.S.C. §112, second paragraph, as being allegedly indefinite for failing to particularly point out and distinctly claim the subject matter applicant regards as the invention.

Claim 12 has been amended so as to provide for antecedent basis in accordance with the Examiners suggestion. Withdrawal of the 35 U.S.C. §112, second paragraph, rejection is respectfully requested.

The 35 U.S.C. §102 Rejection

Claims 1, 3, and 6-8 stand rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Moore et al. (U.S. Pat. No. 5,437,017). This rejection is respectfully traversed.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 869 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). *See also*, M.P.E.P. §2131.

Claim 1 defines a method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data. The computer system includes a main communication network coupled to the plurality of processors. The claimed method includes, among others, generating a TLB message in response to the operation performed on the associated TLB, if (a) a first entry was input into the associated TLB when the corresponding associated physical address was not located; (b) a second entry associated with the corresponding associated physical address was moved to another location within the computer system; or (c) the second entry was removed, as recited in claim 1 as amended.

Moore discloses a method and system for maintaining TLB coherency. The Examiner equates the translation lookaside buffer invalidate (TLBI) instruction of Moore with the TLB message of the claimed invention. However, in Moore, as shown in FIG. 4 thereof and described in column 7, lines 19-25, the TLBI instruction is first placed in the "EXECUTE" position within a processor **10** (see also FIG. 2). Thus, the TLBI

instruction is an instruction (programming command) to be executed by a software program on the processor **10**, and an operation on a TLB is performed after executing the TLBI instruction. Thus, the TLBI instruction of Moore is not a TLB message generated in response to the operation performed on the associated TLB, as claimed in claim 1. In addition, a TLB message of the present invention only includes, for example, a code indicating that it is a TLB message, a read/write bit (may be implicit in the code), and the physical address, but there is no instruction in the TLB message.

Furthermore, in Moore, a unique bus structure is broadcast to a shared bus in response to an execution of the TLBI instructions (see Abstract). However, the TLB message of the claimed invention is generated in response to an actual operation on the TLB (input, modify, or remove of an entry), as recited in claim 1, and not generated as a result of executing a special instruction within the processor as Moore's system does.

Claim 8 includes substantially the same distinctive features as claim 1.

Accordingly, it is respectfully requested that the rejection of claims based on Moore be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

The 35 U.S.C. §103 Rejection

Claims 9-18 stand rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Chan et al. (U.S. Pat. No. 5,524,216) in view of Moore et al. This rejection is respectfully traversed.

According to M.P.E.P. §2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

Claim 9, as amended, defines an electronic data processing apparatus capable of maintaining translation lookaside buffer ("TLB") coherency. The apparatus includes a plurality of processors, and a plurality of TLBs each of which is connected to and associated with a respective processor of the plurality of processors. The claimed apparatus further includes an interconnect network having a plurality of independent paths, each of said plurality of processors distributed among said plurality of independent paths, said plurality of processors being interconnected to each other via corresponding one of said plurality of independent paths, and a TLB message generator provided for each of the plurality of processors, said TLB message generator adapted to determine an accessed data address and generate and transmit a TLB message on corresponding one of said plurality of independent paths, as recited in claim 9, as amended.

Chan teaches a computer system having a multi-tired bus system. Chan's multi-tired bus system includes one or more local buses **20**, **25** and a central bus **10** connected to each local bus by a bus interface **11**, **12** (Abstract, FIG. 1 of Chan). However, as shown in FIG, 1, a processor **21** and a processor **22** are connected to the local bus **20** (column 2, lines 59-61 of Chan), and thus the local bus is still shared by a plurality of processors in Chan. The central bus **10** is shared by all local buses and processors. Therefore, Chan fails to teach or suggest the interconnect network having a plurality of independent paths, the plurality of processors being interconnected to each other via corresponding one of said plurality of independent paths, as recited in claim 9.

Moore teaches generating a TLBI instruction which is broadcast to other processors in a system over a main bus, as the Examiner correctly noted in the Office Action. However, the main bus **8** is of Moore a shared bus which is a single communication path shared among the processors (see FIG. 1 of Moore). For this reason, Moore's system requires a specific arbitration and "RETRY" scheme as described in column 7, line 36 to column 8, line 31 thereof. Since the present invention uses the interconnect network as claimed, no bus arbitration or retry is necessary. In addition, the present invention is more efficient since the present invention does not require executing an instruction, and also the TLB operations in the present invention can be performed in parallel with execution of normal instructions.

Accordingly, Chan, whether considered alone or combined with or modified by Moore, does not teach or suggest the interconnect network as claimed in claim 9. Claim 12 also includes substantially the same distinctive feature as claim 9.

Accordingly, it is respectfully requested that the rejection of claims based on Chan and Moore be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-7 depend from claim 1, claim 10-11 depend from claim 9, and claims 13-18 depend from claim 12, and thus include the limitations of respective independent claims. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Request for Allowance

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Respectfully submitted,
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Limited Recognition under 37 CFR §10.9(b)

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